REMARKS

Applicant is submitting this request for continued examination in order to obtain further consideration of the merits of the claimed invention in view of the cited prior art references. In this regard, Applicant respectfully requests the Examiner to reconsider his assertion that Kanamori discloses "regions **5** ... inside a trench." (Official Action of January 29, 2003, page 5). This assertion is erroneous. The regions **5** in Kanamori represent extrinsic base regions **5** that are electrically connected to an intrinsic base region **3**. However, there is absolutely no trench disclosed by Kanamori. Instead, the regions **5** comprise boron dopants that are diffused from "the high-concentration base polysilicon film (**4a**) ... by a thermal process ..." (See, paragraph 9 of Kanamori). Thus, the regions **5** represent regions that are formed by diffusion, not by any trench formation and fill-in process.

Nonetheless, Applicant acknowledges that FIG. 3 of U.S. Patent No. 5,506,157 to Lee et al. discloses polysilicon regions **24** that operate as "extrinsic base regions." (See, Col. 4, lines 13-15, Lee et al.). A connecting portion **25** is also illustrated in FIG. 3. These connecting portions **25** electrically connect the extrinsic base regions **24** to the intrinsic base region **27** (through a hole in the sidewall oxide layer **34**). Accordingly, even if Lee et al. is combined with Kanamori, as argued by the Examiner, the combination of these references cannot possibly disclose or suggest the subject matter of amended independent Claims 1, 27 or 28.

For example, even if the extrinsic base regions **24** in FIG. 3 of Lee et al. are treated as base electrodes, as argued by the Examiner, there is absolutely no suggestion in the cited prior art of a "trench insulating layer that lines a bottom and sidewalls of said trench and prevents direct electrical contact between the trench-based electrode portion of said base electrode and said extrinsic base region," as recited by Claim 1. (See also, Claim 27). To assist the Examiner, Claim 1 has been annotated with reference numerals to illustrate how it reads on the device illustrated by FIG. 12 of the present application:

1. (Amended) A bipolar junction transistor, comprising:

an intrinsic collector region **13** of first conductivity type in a semiconductor substrate **10**;

a trench in said substrate, adjacent said intrinsic collector region **13**;

a base electrode **79** of second conductivity type in the semiconductor substrate, said base electrode comprising a trench-based electrode portion that extends in said trench and a lateral base electrode extension **79b** that extends outside said trench;

an extrinsic base region **81** of second conductivity type that is self-aligned and electrically connected to said lateral base electrode extension **79b** and forms a P-N rectifying junction with said intrinsic collector region **13**;

an intrinsic base region **83** of second conductivity type that is self-aligned to said lateral base electrode extension **79b**, has a lower second conductivity type doping concentration therein relative to said extrinsic base region **81** and forms a P-N rectifying junction with said intrinsic collector region **13**;

a trench insulating layer **77** that lines a bottom and sidewalls of said trench and prevents direct electrical contact between the trench-based electrode portion of said base electrode **79** and said extrinsic base region **81**; and

an emitter region **89** of first conductivity type that forms a P-N rectifying junction with said intrinsic base region **83**.

Claim 28 also recites many features that are not disclosed or suggested by the cited prior art references. For example, Claim 28 recites many self-aligned features of the claimed transistor that are not disclosed or suggested by the cited prior art. In particular, none of the cited prior art references disclose or suggest an "extrinsic base region that ... is self-aligned to a portion of the polysilicon base electrode that extends into the lateral recess." Thus, it cannot be reasonably maintained that Kanamori and Lee et al. disclose or suggest the subject matter of Claim 28.

Based on these amendments and remarks, Applicant respectfully submits that the present application is in condition for allowance. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "**Version with Markings to Show Changes Made**".

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: BOX RCE, Commissioner for Patents, Washington, DC 20231, on April 24, 2003.

Candi L. Riggs
Candi L. Riggs
Date of Signature: April 24, 2003

Version with Markings to Show Changes Made

In the Claims:

The claims have been amended as follows:

1. (Amended) A bipolar junction transistor, comprising:

an intrinsic collector region of first conductivity type in a semiconductor substrate;

a trench in said substrate, adjacent said intrinsic collector region;

a base electrode of second conductivity type in the semiconductor substrate, said base electrode comprising a trench-based electrode portion that extends in said trench and a lateral base electrode extension that extends outside said trench;

an extrinsic base region of second conductivity type that is self-aligned and electrically connected to said lateral base electrode extension and forms a P-N rectifying junction with said intrinsic collector region;

an intrinsic base region of second conductivity type that is self-aligned to said lateral base electrode extension, has a lower second conductivity type doping concentration therein relative to said extrinsic base region and forms a P-N rectifying junction with said intrinsic collector region;

a trench insulating layer that lines a bottom and sidewalls of said trench and prevents direct electrical contact between the trench-based electrode portion of said base electrode and said extrinsic base region; and

an emitter region of first conductivity type that forms a P-N rectifying junction with said intrinsic base region.

Please cancel Claims 2-4.

5. (Amended) The transistor of Claim 1, **[**2, wherein said base electrode includes a base electrode extension that extends along a surface of said substrate; and**]** wherein said emitter region is self-aligned to a sidewall of the lateral base electrode extension.

6. (Amended) The transistor of Claim 1 **[**4**]**, wherein said trench is ring-shaped; and wherein said extrinsic base region is ring-shaped.

7. (Amended) The transistor of Claim 5, further comprising:

an electrically insulating sidewall spacer on the sidewall of the lateral base electrode extension; and

an emitter electrode of first conductivity type on the surface of said substrate and on said electrically insulating sidewall spacer.

27. (Amended) A bipolar junction transistor, comprising:

an electrically insulating layer on a surface of a semiconductor substrate having an intrinsic collector region of first conductivity type therein, said electrically insulating layer comprising a composite of a first electrically insulating material layer and a second electrically insulating material layer on the first electrically insulating material layer and having a lateral recess therein that extends along an undersurface of the second electrically insulating material layer;

a trench that extends into the surface of the semiconductor substrate and into the intrinsic collector region and is self-aligned to an opening in said electrically insulating layer;

a base electrode of second conductivity type having a first portion that extends in said trench and a second portion that extends into the lateral recess within said electrically insulating layer;

a base region of second conductivity type that is self-aligned and electrically connected to **[a]** the second portion of said base electrode extending into the lateral recess and forms a P-N rectifying junction with said intrinsic collector region;

a trench insulating layer that lines a bottom and sidewalls of said trench and extends between the first portion of said base electrode and said base region so that a direct electrical connection between the first portion of said base electrode and said base region is blocked; and

an emitter region of first conductivity type that forms a P-N rectifying junction with said base region.

28. (Twice Amended) A bipolar junction transistor, comprising:

a semiconductor substrate having an intrinsic collector region of first conductivity type therein that extends to a surface thereof;

an electrically insulating layer on the surface of a semiconductor substrate, said electrically insulating layer having an opening therein and a lateral recess extending from the opening;

a trench that extends into the surface semiconductor substrate and the intrinsic collector region and is self-aligned to the opening in said electrically insulating layer;

a polysilicon base electrode of second conductivity type in the lateral recess and in the trench;

an extrinsic base region of second conductivity type that extends into and forms a P-N junction with the intrinsic collector region and is self-aligned to a portion of the polysilicon base electrode that extends into the lateral recess;

an intrinsic base region of second conductivity type that forms a non-rectifying junction with said extrinsic base region and a P-N rectifying junction with the intrinsic collector region, said intrinsic base region having a lower doping concentration therein relative to said extrinsic base region; and

an emitter region of first conductivity type that extends in the intrinsic collector region.

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